



MODEL ANSWER

WINTER-18 EXAMINATION

Subject Title: Basic Electronics (BEL)

Subject Code:

22216

Important Instructions to examiners:

- 1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
- 2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
- 3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
- 4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
- 5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
- 6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
- 7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q.N.		0.1
		Scheme
	Attempt any FIVE :	10-Total Marks
l)	Draw the symbol of photodiode.	2M
Ans:	Anode Cathode	Correct symbol -2M
))	Define Transistor. State its type.	2M
Ans:	Transistors are active electronic components made of semiconducting materials, which can amplify the electric signals by the application of a small input signal. Types of transistors:	Definition - 1M;
	 Unipolar Junction Transistors Bipolar Junction Transistors 	Types - 1M
e)	Define load and line regulation.	2M
Ans:	 Load regulation is the ability of the power supply to maintain its specified output voltage given changes in the load. Line regulation is the ability of the power supply to maintain its specified output voltage over changes in the input line voltage. 	Each definition - 1M
) Ar :)	ns:	Anode Cathode Define Transistor. State its type. as: Transistors are active electronic components made of semiconducting materials, which can amplify the electric signals by the application of a small input signal. Types of transistors: Unipolar Junction Transistors Bipolar Junction Transistors Bipolar Junction Transistors Define load and line regulation. as: Load regulation is the ability of the power supply to maintain its specified output voltage given changes in the load. Line regulation is the ability of the power supply to maintain its specified output voltage over changes in the input line voltage.

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d)	State application of FET.	2M
Ans	 (NOTE : Any other relevant Application mark shall be given) Applications of FET : As input amplifiers in oscilloscopes, electronic voltmeters and other measuring and testing equipment because high input impedance reduces loading effect to the minimum. Constant current source. They are used to build RF amplifiers in FM tuners and other communication circuits. Because of low noise. FETs are used in mixer circuits of FM and TV receivers as it reduces inter modulation distortion. Used as Analogue switch. As a Valtage Variable Basister (VVP) in constant complifiers 	Any two applications (1M each)
e)	Sketch energy band diagram of semiconductor.	2M
Ans	Energy band diagram for N type semiconductor: Conduction energy band Increased due to destrond Fermi level Valence Energy Band Energy band diagram for P type semiconductor: Conduction Band Fermi level Fermi level Fermi level Threased holes due to acception	Any one correct diagram - 2M

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	f)	State the need of DC regulat	ed power supply.		2M
	Ans:	Need of DC regulated power 1. To convert unregulated AC 2. To convert fluctuating main	supply : into constant DC. supply into regulated constant	nt DC.	Any one relevant need - 2M
	g)	Name the components of fol	lowing symbol:	D S	2M
	Ans:	(i) N-channel Enhancement ty(ii) N-channel Depletion type	rpe MOSFET MOSFET	•	Each correct answer -1M
Q. 2		Attempt any THREE of the	following :	0	12-Total Marks
	a)	Compare PN junction diode	& Zener diode. (four points	3).	4M
	Ans:	Parameter Symbol	PN junction diode	Zener diode	Each point - 1M
		Direction of Conduction	Conducts only in one direction	Conducts in both directions	
		Reverse breakdown	It has no sharp reverse breakdown	It has quite sharp reverse breakdown	
		Application	Used in rectification	Used in regulation	
		Resistance in reverse biased condition	Very high	Very small	
		Characteristics	reverse voltage	Breakdown Voltage, VZ Leakage Current Avalanche Current Reverse Voltage	

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I	b)	Explain with a neat circuit diagram of voltage divider bias method for biasing a	4M
_	•	transistor.	
	Ans:	The voltage divider is formed using external resistors R ₁ and R ₂ . The voltage across R ₂ forward biases the emitter junction. By proper selection of resistors R ₁ and R ₂ , the operating point of the transistor can be made independent of β . In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. The voltage at transistor base, V _B = V _{CC} X $\frac{R_2}{R_1 + R_2}$ Neglecting V _B , The emitter current = I _E = $\frac{V_E}{R_E}$ V _{CE} = V _{CC} - I _C , R _C - I _E , R _E	Explanation - 2M Diagram - 2M
•	2)	Draw the block diagram of DC power supply. Explain the function of each block.	4M
	Ans:	Filter Regulator COutput	Diagram - 2M
		Transformer Transformer : It reduces the amplitude of ac voltage to the desired level and applies it to a rectifier circuit. Rectifier : This circuit converts the voltage at the secondary of the transformer into a pulsating dc voltage. Filter: This circuit reduces the ripple content in the pulsating dc, producing unregulated dc voltage. Regulator: This circuit converts the unregulated dc voltage into regulated constant dc voltage	Functions - 2M
•	d)	Explain the concept of DC load line and oprating point.	4M
	Ans:	DC load line : The straight line drawn on the characteristics of a BJT amplifier which give the DC values of collector current I _C and collector to emitter voltage V _{CE} corresponding to zero signal i.e. DC conditions is called DC load line. To plot I _{C(MAX)} , V _{CE (MAX)} on output characteristics: Get V _{CE (MAX)} by putting I _{c = 0} $V_{CE} = V_{CC} - I_c R_c$ $V_{CE} (MAX) = V_{CC}$ since I _c = 0 Get I _{C(MAX)} by putting V _{CE = 0} Increme = $\frac{V_{CC}}{V_{CE}}$	1M
		$I_{C(MAX)} = \frac{R_{C}}{R_{C}}$	2M
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		MAHARASHTRASTATE BOARD OF TECHNICAL EDUCATION (Autonomous) (ISO/IEC - 27001 - 2013 Certified)	Approacts Degree & Diploma Engineering
		$\begin{array}{c} \hline & & & & \\ \hline & & & \\ I_{C} = & & \\ \hline & & \\ I_{C} = & & \\ \hline & & \\ I_{C} = & & \\ \hline & & \\ \hline & & \\ I_{C} = & & \\ \hline & & \\ \hline & & \\ \hline & & \\ I_{C} = & & \\ \hline & & \\ \hline & & \\ \hline & & \\ \hline & & \\ I_{C} = & & \\ \hline \hline & & \\ \hline & & \\ \hline & & \\ \hline & & \\ \hline \hline & & \\ \hline & & \\ \hline \hline & & \\ \hline \hline & & \\ \hline \hline &$	1M
Q. 3		Attempt any THREE of the following:	12-Total Marks
	a)	An AC supply of 230 V is applied to HWR through a transformer with turns ratio 10:1. Find Average DC output, Voltage current and PIV of diode, RMS value of voltage and current.	4M
	Ans:	Vrms=230V, np/ns=10/1 Max primary voltage is $Vp=\sqrt{2}* Vrms$ $=\sqrt{2}* 230$ =325.22Volt The max secondary voltage is Vm=ns/np*Vp= =1/10*325.22 =32.52V V average=Vdc=Vm/n =32.5/3.14 =10.35V PIV=Vm= 32.52V Vrms=Vm/2 =32.52/2 =32.52/2	Vdc = 1 Mark PIV =
		=16.25V Idc=Im/π Irms= Im/2 Assume RL=10KΩ - (Note - Students may assume any value and attempt to solve, can be considered)	1 Mark

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	$Im=Vm/R_{L}$ =32.52/10 =3.25mA $Idc=Im/\pi$ =3.25*10 =1.03 mA Irms=Im/2 =3.25*11 =1.62 m	0*1000 $10^{-3}/\pi$ A $10^{-3}/2$ hA		Idc = 1 Mark Irms = 1mark
b)	State the va (i) (iii	lues of following parameter Ripple factore (ii) TUF (i	rs with reference to full wave rectifier: i) Efficiency v) P/V	4M
Ans:	(i) (ii) (iii) (iv	Ripple factor -48% Efficiency - 81.2% TUF -69.3 or 81.2 PIV- Vm		1 mark each parameter
c)	Compare E	MOSFET & DMOSFET.		4 M
Ans:	Sr. No. 1	E MOSFET Insulating oxide layer is present between gate and substrate channel is absent. At the operation induced channel get created.	DMOSFET An insulating oxide layer is present between G & channel n or p-type channel is present.	Any 4 points – 1mark each
	2.	For n- channel EMOSFET V_{GS} will be only positive.	For an n-channel DMOSFET, the V _{GS} can be negative for depletion mode & positive for Enhancement mode	
	3	For an n-channel EMOSFET I_D increases as V_{GS} becomes more and more positive	For an n-channel DMOSFET I_D decreased as V_{GS} becomes more and more negative.	
	4	For an n-channel EMOSFET $I_D = 0$ for $V_{GS} \le V_T (V_{GSTh})$	For an n-channel DMOSFET $I_D = 0$ for $ V_{GS} \geq V_P$	

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		$Is=Iz+I_L$ $Iz=Is- I_L$ =0.02 - 0.0008 = 0.0192A iv)Power dissipatt =V_L* I_L = 8* 0.0008 = 0.0064 =6.4mW	ion				Power dissipation = 1mark
Q. 4		Attempt any TH	REE of the fol	lowing:			12-Total Marks
	a)	Compare L, C, I suitability for he	LC and π filter avy / light load	[.] on the basis o l.	f usefulness in reduc	cing ripple or	4M
	Ans:	Parameters Ripple Suitability for heavy / light load.	L filter MORE HEAVY LOAD	C filter LESS LIGHT LC	LC filter LOW DAD HEAVY LOAD CURRENT	n filter LOWEST LOW LOAD CURRENT	ripple or suitability for heavy / light load = 1 mark each point
	b)	Explain the oper	ating principle	e of PNP trans	istor.		4M
	Ans:	A PNP transistor biased battery V_E base (E-B), juncti exceed the barrier transistors. The forward biase in the P type emit	biased in active and the collector on is forward b potential whice ed on the emitted ter region to flo	e mode, i.e. the or – base (C-B) iased only if th h is 0.7 volts for er base (E-B) ju	P o	unction as forward iased, the emitter – 8) voltage (VEB) s for germanium y carriers i.e. holes 'his E-B junction,	Diagram – 1 mark Explanation = 3marks





	Most collector current is also injected current because this current is produced due to the holes injected from the emitter region. There is another small component of collector current due to thermally generated carriers. This current component is called reverse saturation current (I_{CO}) and is quite small. In this way, almost entire emitter current flows in the collector circuit, it is clear that the emitter current is the sum of the base current and collector current i.e. $I_E = I_B + I_C$	
c)	Find the Q point values for the following circuit, Assume $V_{BE} = 0.7 \text{ V} \& \beta = 60$. $R_{B} = 290 \text{ k}\Omega$ $R_{B} = 290 \text{ k}\Omega$ $R_{B} = 60$	4M
Ans:	V _{cc} R _c Saturation point (or upper end) Active region Cut-off point (or lower end) Collector-to-emitter voltage (V _{cc})	
	By KVL $V_{CE}=$ Vcc - Ic.Rc For point on X axis—Ic=0 $V_{CE}=$ Vcc=10V For point on Y AXIS VCE=0 Ic=Vcc/Rc = 10/2000 = 0.005 =5mA	Ic = 2marks V _{CE} = 2marks
d)	Compare BJT & JFET with reference to following point: i) Symbol ii) Transfer characteristics iii) I/P impendence iv) Application	4M













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CONDITION 2. WHEN LOAD RESISTANCE IS REDUCEDWhen load resistance is decreased, the load current increases. This leads to decrease in Iz. Because of this the input current and the voltage drop across series resistance remains constant. Hence the load voltage is also kept constant.12-Total Marks Q.5 Attempt any TWO of the following : a) With neat circuit diagram and mathematical expressions, explain the self-biasing used in F.E.T.6M Ans: I. SELF BIASING • In this circuit there is only one drain supply and no gate supply. • The gate terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected through resistor R6 to the ground. • The source terminal is connected to the sole south is neutrestance of JFET is yery high. Due to this input gate current L0 = zero. Hence if resistor R6 is connected in series with gate terminal. • Vola = Ia R0 = 0Mathematical a expression:2 M• Vola = Ia R0 = 0Vola = - 0 · Vola = - 10 R0 = 0 · Vola = - 10 RS = 0 ·			current I_Z increases. Thus the value of input current and voltage drop across series resistance is kept constant. Hence the load voltage remains constant.	
Q.5When load resistance is decreased, the load current increases. This leads to decrease in Iz. Because of this the input current and the voltage drop across series resistance remains constant. Hence the load voltage is also kept constant.12-Total MarksQ.5Attempt any TWO of the following : a)12-Total Marksa)With neat circuit diagram and mathematical expressions, explain the self-biasing used in F.E.T.6MAns:I. SELF BIASING • In this circuit there is only one drain supply and no gate supply. • The gate terminal is connected through resistor Ro to the ground. • The source terminal is connected through resistor Ro to the ground. • The source terminal is connected through resistor Ro to the ground. • The source terminal is connected IP-IP-IP to the other source is always reverse bias, due to this input resistance of IP-IP is growp the formation and the top of the source is always reverse bias, due to this input resistance of IP-IP is growp the formation and the top of the source is always reverse bias, due to this input resistance of IP-IP is growp the formation and the source is always reverse bias, due to this input resistance of IP-IP is growp the formation and the source is always reverse bias, due to this input resistance of IP-IP is growp the formation and the source is always reverse bias, due to this input source is a source is a source is always reverse bias, due to this input source is a source is a source is always reverse bias, due to this input source is a source is always reverse bias, due to this input source is a source is always reverse bias, due to this input source is a source is always reverse bias, due to this input source is always reverse bias due to this input source is always reverse bias due to this input source is always reverse bias due to this input source i			CONDITION 2. WHEN LOAD RESISTANCE IS REDUCED	
Q.5Attempt any TWO of the following :12-Total Marksa)With neat circuit diagram and mathematical expressions, explain the self-biasing used in F.E.T.6MAns:I. SELF BIASINGIn this circuit there is only one drain supply and no gate supply.6M• In this circuit there is only one drain supply and no gate supply.The gate terminal is connected through resistor R ₀ to the ground. (NOTE: In JFET input PN junction between gate & source is always reverse bias, due to this input resistance of JFET is yetly http: Due to this input gate current Ig = zero. Hence if resistor R ₀ is connected in series with gate terminal, voltage drop across R ₀ is zero as V _{R0} = (TaR ₀ = 0)Mathematic al expression:2•V _G = I _G R _G = 0•V _G = 0V _{R0} = (TaR ₀ = 0)•V _G = I _G R _G = 0•V _{GS} = V _{R0} - V _{SS} = -V _S APPLY KVL TO INPUT LOOP V _{GS} + I _p R _S = 0 · V _{GS} = 0Shockley's equation•APPLY KVL TO OUTPUT LOOP V _{DD} - I _{DRS} = 0 V _{DSQ} = V _{DD} - I _{DRS} = 0			When load resistance is decreased, the load current increases. This leads to decrease in I _Z . Because of this the input current and the voltage drop across series resistance remains constant. Hence the load voltage is also kept constant.	
a)With neat circuit diagram and mathematical expressions, explain the self-biasing used in F.E.T.IntroductionAns:1. SELF BIASINGCircuit Digram:3M•In this circuit there is only one drain supply and no gate supply. • • The gate terminal is connected through resistor RG to the ground. (NOTE: In JEET input PN junction between gate & source is always reverse bias, due to this input resistor RG is connected in series with gate terminal, voltage drop across RG is zero as VRG = $10^{10} R_{\odot} = 0$ Circuit Digram:3M Explanation: 1M Mathematical expression:2 M•VG = IG RG = 0VG = U = VS $= -VS$ APPLY KVL TO INPUT LOOP VGS + IpRS = 0 $: VGS = -IpRS$ Shockley's equation $: Ib = lbsS (1 \frac{V_{SS}}{V_{SS}})^2$ Shockley's equation $: Ib = lbsS (1 \frac{V_{SS}}{V_{SS}})^2$ •APPLY KVL TO OUTPUT LOOP VDS - JDRD - J	Q.5		Attempt any TWO of the following :	12-Total Marks
Ans: I. SELF BIASING I. SELF BIASING I. In this circuit there is only one drain supply and no gate supply. The gate terminal is connected through resistor R _i to the ground. The source terminal is connected through resistor R _i to the ground. (NOTE: In JFET input PN junction between gate & source is always reverse bias, due to this input resistance of JFET is yers high. Due to this input gate current I _G = zero. Hence if resistor R _G is connected in series with gate terminal, voltage drop across R _i is zero as V _{RG} = 16 R _G = 0} V _G = I _G R _G = 0 V _{GS} = V _G - V _S = -V _S APPLY KVL TO INPUT LOOP V _{GS} + I _D R _S = 0 \therefore V _{GS} = -I _D R _S I. D = I _{DSS} (1 - $\frac{V_{GS}}{V_p}$) ² Shockley's equation APPLY KVL TO OUTPUT LOOP V _{DSQ} = V _{DD} - U _{DSQ} - I _D R _S = 0 V _{DSQ} = V _{DD} - U _{DSQ} - I _D R _S = 0		a)	With neat circuit diagram and mathematical expressions, explain the self-biasing used in F F T	6M
		Ans:	 used in F.E.T. 1. SELF BIASING In this circuit there is only one drain supply and no gate supply. The gate terminal is connected through resistor R₀ to the ground. (NOTE: In JFET input PN junction between gate & source is always reverse bias, due to this input resistance of JFET is yery high? Due to this input gate current I₀ = zero. Hence if resistor R₀ is connected in series with gate terminal, voltage drop across R₀ is zero as V_{RG} = fo R₀ = 0 V_G = I_G R_G = 0 V_G = I_G R_G = 0 V_{GS} = V_G - V_S = -V_S APPLY KVL TO INPUT LOOP V_{GS} + I_DR_S = 0 : V_{GS} = -I_DR_S I_D = I_{DS} {1 ^LC_S/V_P } Shockley's equation APPLY KVL TO OUTPUT LOOP V_{DD} - I_DR_D - V_{DSQ} - I_DR_S = 0 V_{DSQ} = V_{DD} - I_DR_D - I_DR_S 	Circuit Digram:3M Explanation: 1M Mathematic al expression:2 M

















ADV A	NTAGES : (Any Two Points)	
•	 Efficiency: LEDs emit more lumens per watt than incandescent light bulbs. Color: LEDs can emit light of an intended color. This is more efficient and can lower initial costs. Size: LEDs can be very small (smaller than 2 mm²) and are easily attached to printed circuit boards. On/Off time: LEDs light up very quickly. LEDs used in communications devices can have even faster response times. Dimming: LEDs can very easily be dimmed either by pulse-width modulation or lowering the forward current. Cool light: In contrast to most light sources, LEDs radiate very little heat. Slow failure: LEDs mostly fail by dimming over time, rather than the abrupt failure of incandescent bulbs. Lifetime: LEDs can have a relatively long useful life product 	Advantages 1M (2Points)
•	Shock resistance: LEDs, being solid-state components, are difficult to damage with external shock, unlike fluorescent and incandescent bulbs, which are fragile.	
•	Focus: The solid package of the LED can be designed to focus its light. Disadvantages (Any Two Points):	
• • • • • • • •	 High initial price: LEDs are currently more expensive (price per lumen) on an initial capital cost basis, than most conventional lighting technologies. Temperature dependence: LED performance largely depends on the ambient temperature of the operating environment – or "thermal management" properties. Voltage sensitivity: LEDs must be supplied with the voltage above the threshold and a current below the rating. Current and lifetime change greatly with a small change in applied voltage. Light quality: Most cool-white LEDs have spectra that differ significantly from a black body radiator like the sun or an incandescent light. Area light source: Single LEDs do not approximate a point source of light giving a spherical light distribution. Efficiency droop: The efficiency of LEDs decreases as the electric current increases. Heating also increases with higher currents which compromise the lifetime of the LED. Impact on insects: LEDs are much more attractive to insects. Use in winter conditions: Since they do not give off much heat in comparison to traditional electrical lights, LED lights used for traffic control can have snow obscuring them, leading to accidents. 	Disadvantag es: 1M (2Points)
<u>Ap</u> • •	 oplications of LED (Any Two Points):: As a power indicator. In seven segment display. In the opto-couplers. In the infrared remote controls. 	Application 1M (2Points)





braw circuit and describe working of full wave rectilier using center tapped transformer with waveforms	0101
Full wave Rectifier with Center tanned transformer(FWR):	
• In full wave rectification, the rectifier conducts in both the cycles as two diodes	Circuit Diagram:2
are connected.	M
<u>Circuit diagram:</u>	
 Circuit diagram: Ac voltage The circuit employs two diodes D1 and D2 as shown. A center tapped secondary winding AB is used with two diodes connected. So that each uses one half - cycles of input AC voltage. Diode D1 utilized the AC voltage appearing across the upper half (OA), while diode D2 uses the lower half winding (OB). The voltage V_s between the center-tap and either ends of secondary winding is half of the secondary voltage V₂ i.eV_s = V₂/2. If the output voltage should be equal to the input voltage, a step up transformer with turns ratio N₁/N₁ = 2 must be used. Thus the total secondary voltage V₂ is twice the primary voltage. i.e., V_s = V₁ = V₂/2. Operation: The end A of the secondary winding becomes positive and end B negative. This makes diode D1 forward biased and diode D2 reverse biased. Therefore D1 conducts while D2 does not. The conventional current flow direction in the upper half winding as shown in th fig above. A – D1 – RL – O In negative half cycle (II-2II): End A of secondary winding becomes negative and end B positive. Therefore diode D2 conducts while diode D1 does not. 	P Description 2M
• The conventional current flow is from as shown by the arrows in the above fig. B - D2 - RL - O	
 From fig. current in the load RL is in the same direction for both half-cycles of input AC voltage. Therefore DC is obtained across the load RL. 	





c)i)In CE configuration if $\beta = 99$ leakage current I $cxo = 50 \ \mu$ A. If base current is 0.5 mA. Determine I _C and I _E . ii)6MAns:i)Given: $\beta = 99$ $I_{CEO} = 50 \ \mu$ A, $I_{E} = 0.5 \ m$ A, $= 500 \ \mu$ ATo find I _C and I _E = 1/5marks eachTo Find: I _C $\alpha \neq 1$ IE Solution: I _C $\alpha \neq 99 \ x > 500 \ \mu$ ATo find: IC $\alpha \neq 1$ IE Solution: I _C $\alpha \neq 99 \ x > 500 \ \mu$ ATo find: IC $\alpha \neq 1$ IE BDerive relation between $\alpha \& \beta$ Therefore, I _C $\alpha \neq 99 \ x > 500 \ \mu$ ATo E mAIE $\alpha \neq 1$ IF IE IE IC $\alpha \neq 1$ IE I		v_{s} V_{m} V_{m} v_{L} v_{L} V_{m} V_{m} V_{m} V_{m} $Dl \text{ conducts}$ $D2 \text{ conducts}$ $D1 \text{ conducts}$ 2π 3π ωt	Waveforms: 2M
i) Derive relation between $\alpha \& \beta$. Ans: i) Given: $\beta = 99$ $I_{CRO} = 50 \ \mu\text{A},$ $I_B = 0.5 \ \text{mA}, = 500 \ \mu\text{A}$ To Find: $I_C \& I_E$ Solution: $I_C = \beta * I_B + I_{CEO}$ Therefore, $I_C = 99 \ x \ 500 \ \mu\text{A} + 50 \ \mu\text{A}$ $I_C = 49550 \ \mu\text{A}$ Therefore, $IC = 49.55 \ \text{mA}$ $I_B = I_C + I_B$ $I_E = 50.05 \ \text{mA}$ ii) Relation between $\alpha \& \beta$: We know that: $I_E = I_B + I_C(i)$ Dividing equation (i) by I_C . $I_E / I_C = I_B / I_C + I_C / I_C$	c)	i) In CE configuration if $\beta = 99$ leakage current I _{CEO} = 50 µA. If base current is 0.5 mA . Determine I _G and I _E	6M
Ans:i)Given:To find Ic and IE = 1/Smarks each $\beta = 99$ $I_{CE} = 50 \ \mu A$, $I_{B} = 0.5 \ m A_{*} = 500 \ \mu A$ Derive relationTo Find: $I_{C} \ll I_{E}$ $I_{C} \ll I_{E}$ Solution: $I_{C} = \beta * I_{B} + I_{CEO}$ Derive relationTherefore, $I_{C} = 99 \ x 500 \ \mu A + 50 \ \mu A$ Derive relationTherefore, $I_{C} = 99 \ x 500 \ \mu A + 50 \ \mu A$ Derive relationTherefore, $I_{C} = 99 \ x 500 \ \mu A + 50 \ \mu A$ Derive relationTherefore, $I_{C} = 49550\mu A$ Derive relationTherefore, IC = 49.55 \mathcal{Therefore}, IC = 10.5 \mathcal{Therefore}, IC = 10		ii) Derive relation between α & β.	
Therefore $1/\alpha = 1/\beta + 1$ (Since $\alpha = I_C / I_E$, $\beta = I_C / I_B$	Ans:	i) Given: $\beta = 99$ $I_{CEO} = 50 \ \mu\text{A},$ $I_B = 0.5 \ \text{mA}, = 500 \ \mu\text{A}$ To Find: $I_C \& I_E$ Solution: $I_C = \beta * I_B + I_{CEO}$ Therefore, $I_C = 99 \ x \ 500 \ \mu\text{A} + 50 \ \mu\text{A}$ $I_C = 49550 \ \mu\text{A}$ Therefore, $IC = 49.55 \ \text{mA}$ $I_E = 1C + I_B$ $I_E = 49.55 \ \text{mA} + 0.5 \ \text{mA}$ $I_E = 50.05 \ \text{mA}$ ii) Relation between a & \beta: We know that; $I_E = I_B + I_C \dots (i)$ Dividing equation (i) by I_C . $I_E / I_C = I_B / I_C + I_C / I_C$ Therefore $1/a = 1/\beta + 1$ (Since $a = I_C / I_E$, $\beta = I_C / I_B$	To find Ic and I _E = 1/5marks each Derive relation between α & β = 3marks





Therefore $1/\alpha = \underline{1+\beta}$ β Therefore $\alpha = \underline{\beta}$ $1+\beta$ $\alpha(1+\beta) = \beta$ $\alpha + \alpha\beta = \beta$ Therefore $\alpha = \beta - \alpha \beta$ Therefore $\alpha = \beta (1 - \alpha)$ Therefore $\beta = \frac{\alpha}{1-\alpha}$

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